TRANSMITTAL FORM (to be used for all correspondence after initial	Filing Date First Named Inventor Art Unit Examiner Name	Approved for use through 04/30/2003. OMB 0681-0031 and Trademark Office; U.S. DEPARTMENT OF COMMERCE of information unless it displays a valid OMB control number. 10/735,355 Dec. 12, 2003 Zhongze Wang 2812 J. Kennedy MI22-2457
Total Number of Pages in This Submission		
	ENCLOSURES (Check all that a	apply) After Allowance Communication
Fee Transmittal Form Fee Attached Amendment/Reply After Final Affidavits/declaration(s) Extension of Time Request Express Abandonment Request Information Disclosure Statement Certified Copy of Priority Document(s) Response to Missing Parts/ Incomplete Application Response to Missing Parts under 37 CFR 1.52 or 1.53	Drawing(s) Licensing-related Papers Petition Petition to Convert to a Provisional Application Power of Attorney, Revocation Change of Correspondence Addres Terminal Disclaimer Request for Refund CD, Number of CD(s) Remarks Additional Enclosure: A \$180.00 Check	to a Technology Center (TC) Appeal Communication to Board of Appeals and Interferences Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) Proprietary Information
	TURE OF APPLICANT, ATTORNE	Y, OR AGENT
Firm or Mark S. Matkin, Reg. No. Wells St. John, P.S. Signature Date	32,268 57 4/15/05	
C	ERTIFICATE OF TRANSMISSION/	MAILING
I hereby certify that this correspondence is being fa	acsimile transmitted to the USPTO or deposited with nissioner for Patents, Washington, DC 20231 on this	th the United <u>States Postal Service with sufficient</u> postage as is date:

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

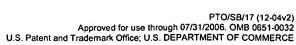
Date

4-14-05

Typed or printed

Signature

Jim Tidrick



APR 1 4 2005 33

## # 108/2004.		Complete if Known
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).	Application Number	10/735,355
FEE TRANSMITTAL	Filing Date	12/12/2003
For FY 2005	First Named Inventor	Zhongze Wang
Applicant claims small entity status. See 37 CFR 1.27	Examiner Name	J. Kennedy
	Art Unit	2812
TOTAL AMOUNT OF PAYMENT (\$) 180.00	Attorney Docket No.	MI22-2457
METHOD OF PAYMENT (check all that apply)		
Check Credit Card Money Order Non	e Other (please id	entify):
Deposit Account Deposit Account Number: 23-0925		
For the above-identified deposit account, the Director is her	· ·	
Charge fee(s) indicated below	Charge fee(s)	indicated below, except for the filing fee
Charge any additional fee(s) or underpayments of fee	e(s) Credit any ov	erpayments
under 37 CFR 1.16 and 1.17 WARNING: Information on this form may become public. Credit card info	ormation should not be inc	cluded on this form. Provide credit card
information and authorization on PTO-2038.		
FEE CALCULATION		
1. BASIC FILING, SEARCH, AND EXAMINATION FEES FILING FEES SEAR	.CH FEES EXA	MINATION FEES
Small Entity	Small Entity	Small Entity
Application Type Fee (\$) Fee (\$) Fee (\$)		
Utility 300 150 500	250 200	
Design 200 100 100	50 130	
Plant 200 100 300	150 160	
Reissue 300 150 500	250 600	
Provisional 200 100 5 4 9	5 7 2 0 9 5	9, 0
2. EXCESS CLAIM FEES Fee Description		Small Entity Fee (\$) Fee (\$)
Each claim over 20 (including Reissues)		50 25
Each independent claim over 3 (including Reissues)		200 100 360 180
Multiple dependent claims Total Claims Extra Claims Fee (\$) Fee	Paid (\$)	360 180 Multiple Dependent Claims
- 20 or HP = x =	<u>ι αια (φ)</u>	Fee (\$) Fee Paid (\$)
HP = highest number of total claims paid for, if greater than 20.		
	Paid (\$)	
3 or HP = x = HP = highest number of independent claims paid for, if greater than 3.		
3. APPLICATION SIZE FEE If the specification and drawings exceed 100 sheets of par	ner (excluding electror	nically filed sequence or computer
listings under 37 CFR 1.52(e)), the application size fee		
sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G)	and 37 CFR 1.16(s).	
	h additional 50 or frácti (round up to a whole ni	
4. OTHER FEE(S) Non-English Specification, \$130 fee (no small entity of		Fees Paid (\$)
Other (e.g., late filing surcharge): Supplemental Information	*	\$180.00
SUBMITTED BY	Registration No. 32 268	Telephone 509-624-4276

SUBMITTED BY		
Signature	Registration No. (Attorney/Agent) 32,268	Telephone 509-624-4276
Name (Print /Type)	Mark S. Matkin	Date 4-15-05

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

ED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	10/735,355
Filing Date	
Inventorship	Zhongze Wang
Assignee	Micron Technology, Inc.
Group Art Unit	
Examiner	J. Kennedy
Attorney's Docket No	MI22-2457
TitleWafer Bonding Method of Forming	Silicon-On-Insulator Comprising
Integrated Circuitry	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. Copies of the cited art are not included (1276 Off. Gaz. Pat. Off 55, 05 August 2003). No admission is made regarding whether all the submitted references are prior art.

EV549572093

Respectfully submitted,

Dated: 4-15-05

Reg. No. 32,268

04/18/2005 MBIZUNES 00000032 10735355 180.00 OP 01 FC:1806

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. MI22-2457

SERIAL NO. 10/735,355

if necessary)

APPLICANT: Zhongze Wang

Use several sheets if necessary)

FILING DATE December 12, 2003 GROUP 2811

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,048,411	4/2000	Henley et al.			
	AB	6,071,783	6/2000	Liang et al.			
	AC	6,091,076	7/2000	Deleonibus			
-	AD	6,245,729	2/2002	Maszara			
	AE	6,346,729	2/2002	Liang et al.			
	AF	6,358,791	3/2002	Hsu et al.	Q F	72	005
	AG	6,403,485	6/2002	Quek et al.	7 0		
	АН	6,649,959	11/2003	Hsu et al.			
	Al	6,664,146	12/2003	Yu			
	AJ	2002/004884	4/2002	Sakaguchi			
	AK	2002/0034844	3/2002	Yusukawa			
	AL	10/924,776		Ford			08/25/2004

OTHER RE	FERENCE	ES (including Author, Title, Date, Pertinent Pages, Etc.)
	АМ	Bashir et al., Characterization of sidewall defects in selective epitaxial growth of silicon, 13 J. VAC. Sci.
		TECHNOL. B, No. 3, pp. 923-927 (May/June 1995).
	AN	Bashir et al., Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in
		silicon selective epitaxial growth, 18 J. Vac. Sci. Technol. B, No. 2, pp. 695-699 (March/April 2000).
	AO	Hammad et al., The Pseudo-Two-Dimensional Approach to Model the Drain Section in SOI MOSFETs,
		48 IEEE TRANSACTIONS ON ELECTRON DEVICES, No. 2, pp. 386-387 (February 2001).
	AP	Sivagnaname et al., Stand-by Current in PD-SOI Pseudo-nMOS Circuits, IEEE, pp. 95-96 (2003)
	AQ	Wang et al., Achieving Low Junction Capacitance on Bulk SI MOSFET Using SDOI Process, Micron Technology, Inc., 12 pages (pre-2004).
EXAMINER		DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.